

**REMARKS**

Reconsideration of the present application, in view of the following remarks, is respectfully requested. Claims 1-6, 8-36, and 38-40 remain pending in the present application.

Claims 1-4, 6, 9-15, 17, 21-23, 25-26, 28-36, and 39-40 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,870,670 to Ripley ("Ripley") in view of U.S. Patent No. 6,304,751 to King ("King"). Claim 1 recites, in part, the features of "a first amplitude detector for determining the amplitude of the output I signal" and "a second amplitude detector for determining the amplitude of the output Q signal." Similarly, claim 22 recites, in part, the steps of "determining the amplitude of the output I signal" and "determining the amplitude of the output Q signal." Claims 34, 39, and 40 recite, in part, the feature of "first and second input terminals for receiving an input signal and producing an output in-phase (I) signal and an output quadrature (Q) signal."

In contrast, King teaches sending the I and Q signals through a pair of matched low pass filters and analog to digital converters 110 at the front end of a digital processing section of the system. See Figure 2 and col. 3, lines 5-9 of King. King merely discloses an error calculation circuitry for determining an error between the I and Q paths, for example through a digital subtraction operation. See col. 4, lines 7-12 of King. As such, King does not disclose the presence of first and second amplitude detectors as recited in claim 1.

Furthermore, as stated by MPEP 2143.01, "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." As noted below, Ripley may not be adapted to use the circuit disclosed by King. King relates to a digital system that may not be utilized in the analog system disclosed in Ripley.

King refers to "moving the zero of the FIR filter 202" at col. 3, lines 58-64, which is a typical realization for a digital circuit which is not possible in analog circuits. Ripley relates to the type of image reject circuit discussed in the background art section of the present application, whereby a phase shifting network in the IF stage is complemented by a phase shifting network in the LO stage. Ripley therefore includes the drawbacks mentioned on page 2 of the present

application, in that two phase shifting networks are needed, and that the components of the phase shifting network in the IF stage needs to be extremely accurate, resulting in the manufacturing disadvantages mentioned on page 1 of the present application. Indeed, these disadvantages are explicitly mentioned in Ripley, where col. 2, lines 56-62 state that “if the image reject mixer is produced with tight matching tolerances...the feedback control signal can control both shifting networks to maintain accurate ninety-degree phase differences.” The phase comparison method in Ripley relies on a constant amplitude in the LO path, i.e., where the phase shifting network resides. See col. 1, line 1 - col. 2 of Ripley. We respectfully submit that Ripley and King are not combinable and Ripley teaches away from using an amplitude difference to determine a tuning signal. As such, claims 1, 22, 34, 39, and 40 distinguish over Ripley and King and Applicants respectfully request that the §103 rejection be withdrawn.

Claims 2-4, 6, 9-15, 17, and 21 are either directly or indirectly dependent from claim 1 and should distinguish over Ripley and King for at least the same reasons as stated above. Claims 23, 25-26, and 28-33 are either directly or indirectly dependent from claim 22 and should distinguish over Ripley and King for at least the same reasons as stated above. Claims 35-36 are directly dependent from claim 34 and should distinguish over Ripley and King for at least the same reasons as stated above. Applicants respectfully request that the §103 rejection of claims 2-4, 6, 9-15, 17, 21, 23, 25-26, 28-33, and 35-36 be withdrawn.

Claims 5, 11, and 24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Ripley in view of King and WO 99/16179 to Moore et al (“Moore”). Claims 5, 11, and 24 are either directly or indirectly dependent from claim 1 or claim 22 and should distinguish over Ripley and King for at least the same reasons as set forth above. Moore does not remedy the deficiencies of Ripley and King in that Moore also does not teach or suggest determining the amplitude of the output I signal and determining the amplitude of the output Q signal as recited in claims 1 and 22. Applicants respectfully submit that claims 5, 11, and 24 distinguish over Ripley, King, and Moore and request that the §103 rejection of claims 5, 1, and 24 be withdrawn.

Claims 8, 16, 18-20, 27, and 38 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Ripley in view of King and U.S. Patent No. 6,226,509 to Mole (“Mole”).

Claims 8, 16, 18-20, 27, and 38 are either directly or indirectly dependent from claim 1, 22, or 34 and should distinguish over Ripley and King for at least the same reasons as set forth above. Mole does not remedy the deficiencies of Ripley and King in that Mole also does not teach or suggest determining the amplitude of the output I signal and determining the amplitude of the output Q signal as recited in claims 1 and 22. Furthermore, Mole does not teach or suggest first and second input terminals for receiving an input signal and producing an output in-phase (I) signal and an output quadrature (Q) signal as recited in claim 34. Applicants respectfully submit that claims 8, 16, 18-20, 27, and 38 distinguish over Ripley, King, and Mole and request that the §103 rejection of claims 8, 16, 18-20, 27, and 38 be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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